#5 Election 7-2-03 ORY

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Scot A. Kellar et al.
Serial No.:	10/066,643
Filed:	February 6, 2002
For:	WAFER BONDING FOR 3-D INTEGRATION
Art Unit:	2823
Examiner:	Michelle ESTRADA

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

June 25, 2003

Sir:

In response to the Restriction Requirement (Paper No. 4) dated on June 16, 2003, Applicants hereby elect, without traverse, Group I (claims 1-7 and 15-20).

REMARKS

Claims 1-20 are pending in this application.

In response to the restriction requirement (Paper No. 4), in which the Examiner indicates that two groups of inventions are being claimed; namely Group I (claims 1-7 and 15-20) drawn to a semiconductor device, allegedly classified in class 257, subclass 737 and Group II (claims 8-14) drawn to a method of making a semiconductor device, allegedly classified in class 438, subclass 118, Applicants respectfully elect, without traverse, the invention of Group I directed to claims 1-7 and 15-20. Non-elected Group II, drawn to claims 8-14, will be reinstated in a divisional application in due course.